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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,399	12/11/2003	Teruyuki Maeda	60437 (70820)	2109

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EXAMINER	
PHAM, LONG	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/735,399	MAEDA, TERUYUKI	
	Examiner	Art Unit	
	Long Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in combination with Williams et al. (US patent 5,648,281).

With respect to claims 1, 3, 6, and 8, AAPA teaches a power transistor comprises of (see figs. 3-5 and associated text of the specification of this application):

a plurality of vertical PNP transistors formed on a P-type silicon substrate 101, the vertical PNP transistors have an N+type electrode layer 108;

a plurality of electrode portions 118 of an N+ buried layer 102 formed to isolate the P-type silicon substrate and the plurality of vertical PNP transistors from each other, wherein the electrode portions are provided on the N+ buried layer and formed of an N+ type electrode layer for making ohmic contact;

AAPA fails to teach an N+ type diffusion layer is formed contacting and surrounding a portion of the N+ type electrode layer, and extending to contact N+ type buried layer.

Williams et al. teach an vertical PNP transistor in which an N+ type diffusion layer 348 is formed contacting and surrounding a portion of an N+ type

electrode layer, and extending to contact an N+ type buried layer 340. See figs. 28 and 28A and col. 24, lines 1-60.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Williams et al. into the device of AAPA to reduce collector resistance. See figs. 28 and 28A and col. 24, lines 1-60.

With respect to claim 5, Williams et al. further teach that the diffusion layer 348 is more doped than the N epitaxial layer, but fail to teach the range for the concentration of the diffusion layer 348. See figs. 28 and 28A and col.24, lines 1-60.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value or range for the concentration of the N+ diffusion layer through routine experimentation and optimization to obtain optimal or desired device performance because absence unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

With respect to claim 4, AAPA further teaches an N + type base well layer 108 as a base region of the plurality of vertical pnp transistor. See figs. 3-5 and associated text of the specification of this application.

Further with respect to claim 4, the process limitation that the N + type diffusion layer and the N + type base well layer are formed at the same time is not given weight in the patentability determination of present device claims.

With respect to claim 2, AAPA further teaches at least part of the electrode portion is provided under common emitter metal lines 109 of the power transistor routed on the active region of the power transistor. See figs. 3-5

and associated text of the specification of this application.

With respect to claim 7, AAPA further teaches the singularity or plurality of electrode portions are placed so as to be uniformly spaced from their respectively adjacent electrode portions. See figs. 3-5 and associated text of the specification of this application.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in combination with Williams et al. (US patent 5,648,281).

With respect to claim 9, AAPA teaches a power transistor comprising (see figs. 3-5 and associated text of the specification of this application):

a plurality of vertical pnp transistors formed on a P-type substrate, each pnp transistor having a P + type collector 106, an N +type base well formed in a base region, a P + type emitter layer 107 and an N + type base layer;

P+ type collector buried layers 103 formed under the N+ type base well;

an N + type buried layer 102 isolating the P-type substrate from the P +type collector;

an N type epitaxial layer 104 formed over a surface of the P type substrate; and

an N + type electrode layer 118.

AAPA further teaches that the electrode portions 118 are provided on the N + buried layer 102, however, AAPA fails to teach an N+ type diffusion layer is formed connecting the electrode portion and the N + buried layer 102 and the N+ type diffusion layer surrounding the electrode portion.

Williams et al. teach an vertical pnp transistor in which a N + diffusion layer 348 is formed connecting electrode portion and N + buried layer and the N+ diffusion layer surrounding the electrode portion. See figs. 28 and 28A and col. 24, lines 1-60.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to form a plurality of N + type diffusion layers as taught by Williams et al. in the device of AAPA to reduce the collector resistance. See figs. 28 and 28A and col.24, lines 1-60.

Further with respect to claim 9, since AAPA in combination with Williams et al. teach the claimed device, at least one of the N+ diffusion layers passes between the P+ type collector buried layers.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Long Pham

Primary Examiner

Art Unit 2814

LP